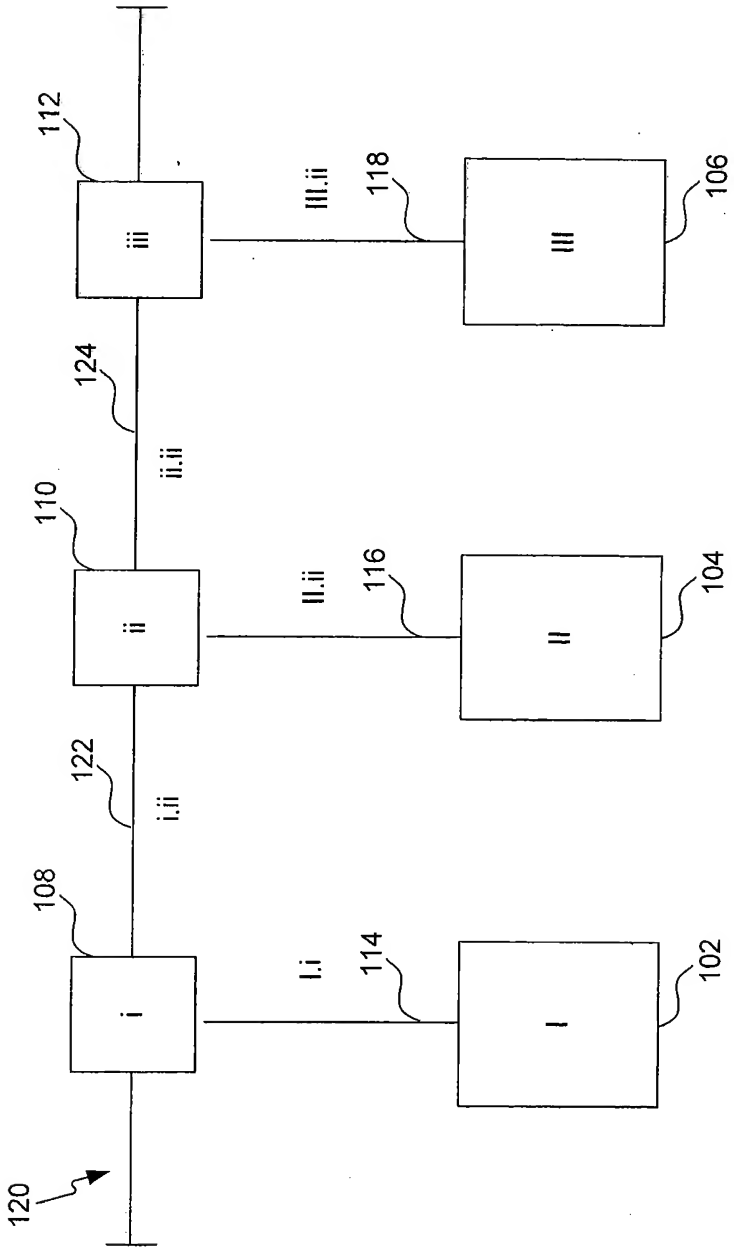
100
112
iii
III.ii
118
III
106
124
ii.ii
110
ii
II.ii
116
II
104
122
i.ii
108
i
I.i
114
I
102
120

FIG. 1

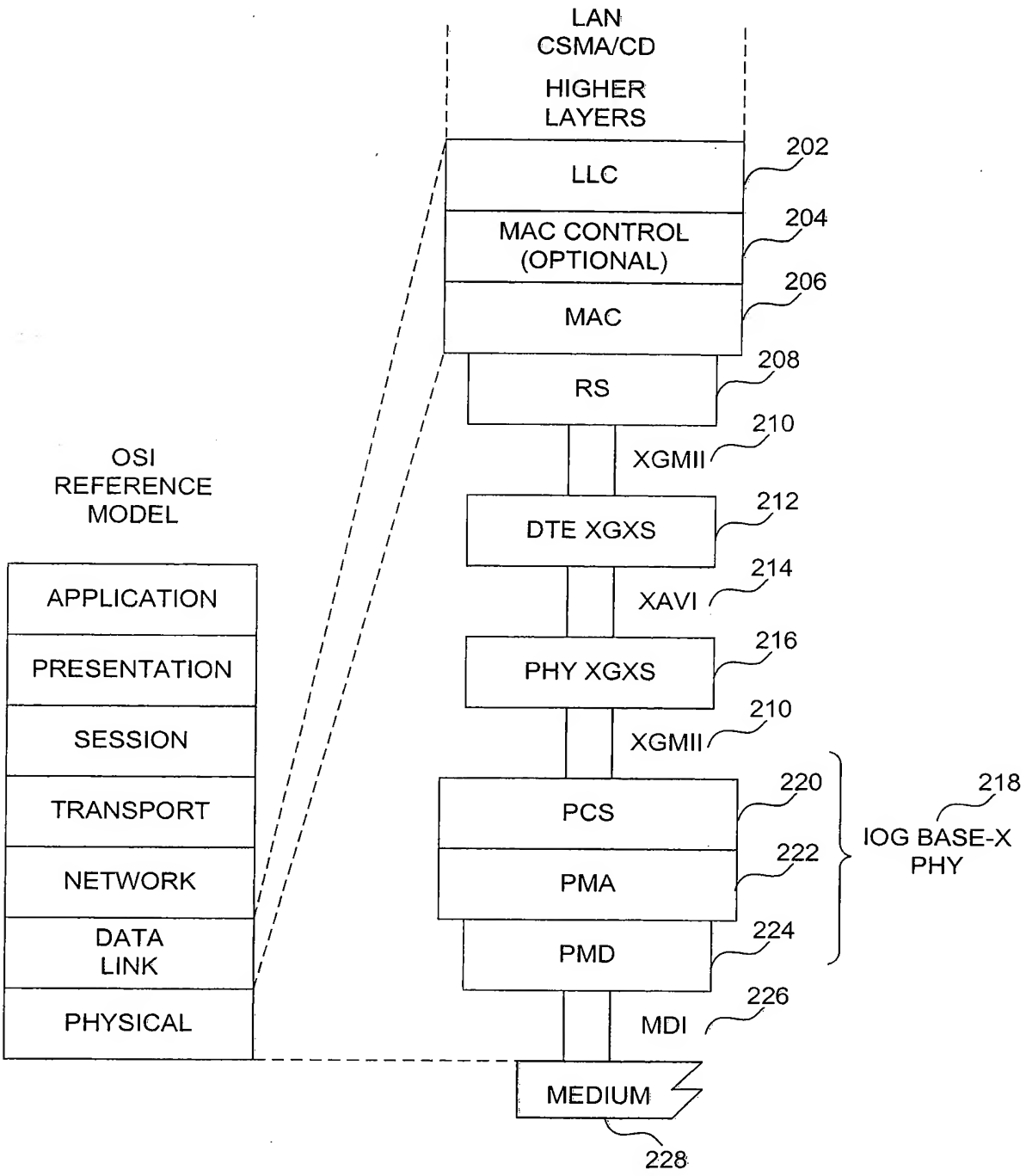
200
LAN
CSMA/CD
HIGHER
LAYERS
LLC
202
MAC CONTROL
(OPTIONAL)
204
MAC
206
RS
208
XGMII
210
DTE XGXS
212
XAVI
214
PHY XGXS
216
XGMII
210
PCS
220
PMA
222
PMD
224
10G BASE-X
PHY
218
MDI
226
MEDIUM
228
OSI
REFERENCE
MODEL
APPLICATION
PRESENTATION
SESSION
TRANSPORT
NETWORK
DATA
LINK
PHYSICAL

FIG. 2

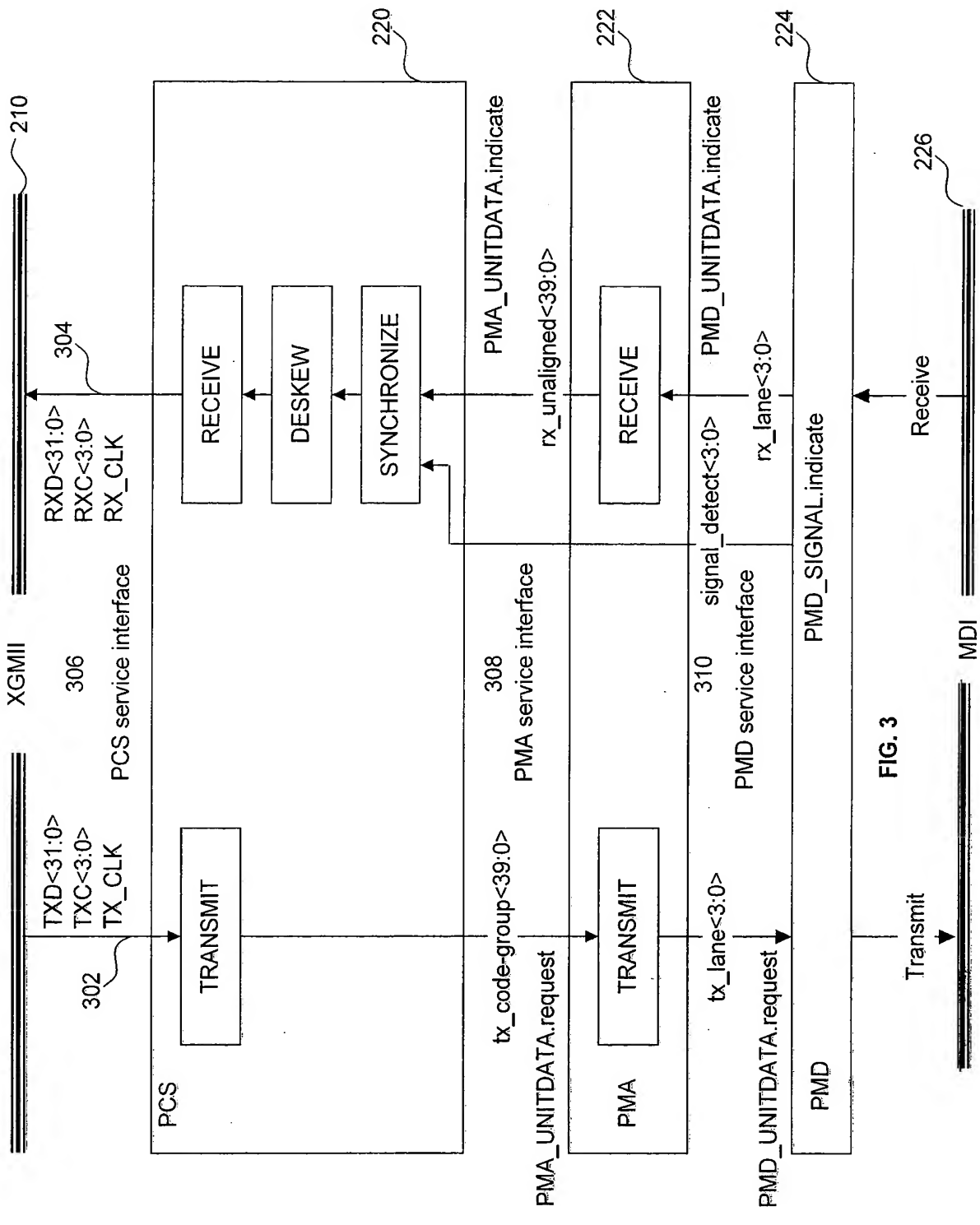
210
XGMII
304
RXD<31:0>
RXC<3:0>
RX_CLK
220
222
224
226
RECEIVE
DESKEW
SYNCHRONIZE
PMA_UNITDATA.indicate
rx_unaligned<39:0>
RECEIVE
PMD_UNITDATA.indicate
rx_lane<3:0>
Receive
306
PCS service interface
308
PMA service interface
310
signal_detect<3:0>
PMD service interface
PMD_SIGNAL.indicate
TXD<31:0>
TXC<3:0>
TX_CLK
302
TRANSMIT
tx_code-group<39:0>
TRANSMIT
tx_lane<3:0>
Transmit
MDI
PCS
PMA_UNITDATA.request
PMA
PMD_UNITDATA.request
PMD

FIG. 3

FIG. 3

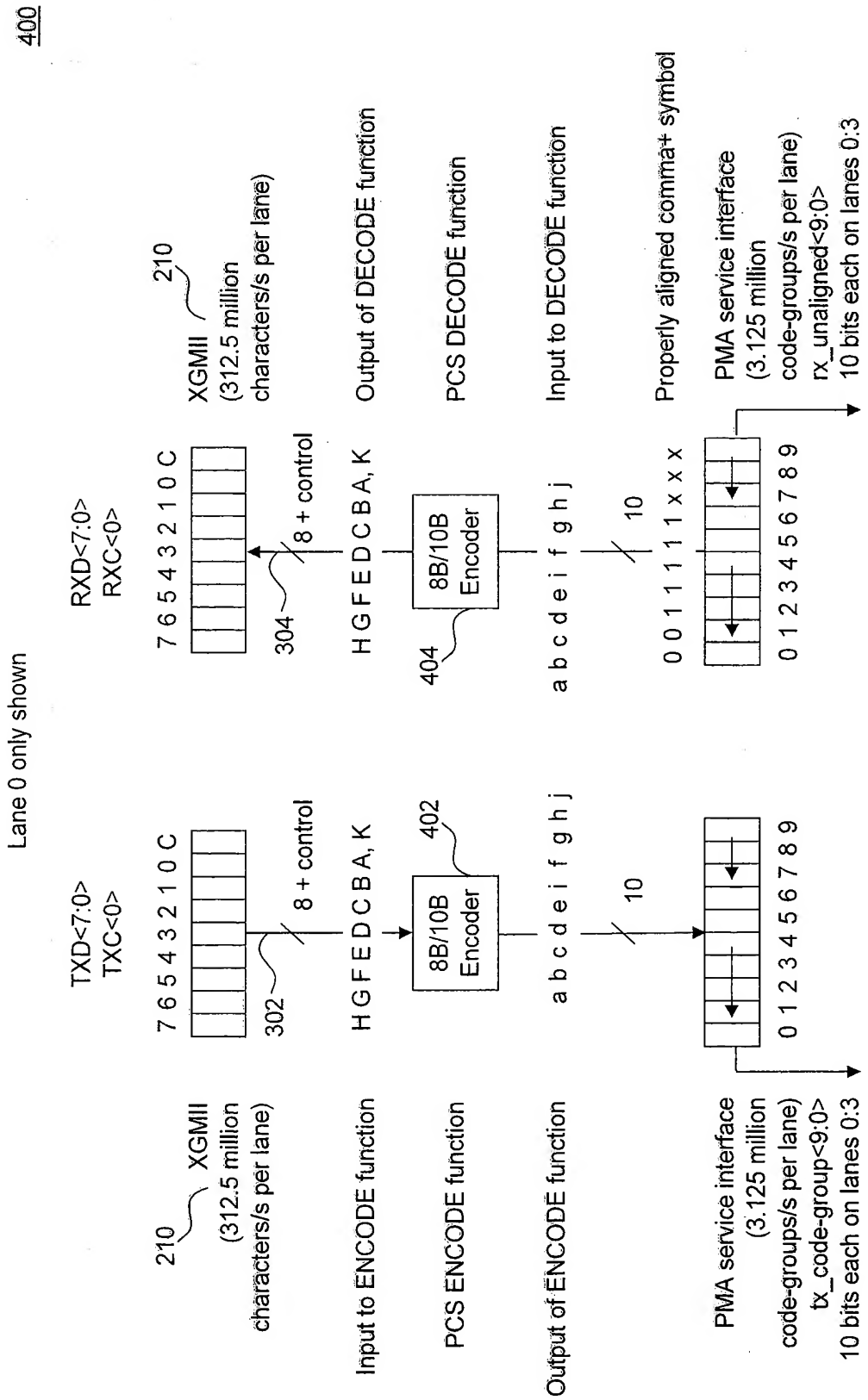
400
Lane 0 only shown
TXD<7:0>
TXC<0>
RXD<7:0>
RXC<0>
210
XGMII
(312.5 million
characters/s per lane)
7 6 5 4 3 2 1 0 C
302
8 + control
304
H G F E D C B A, K
Input to ENCODE function
PCS ENCODE function
8B/10B
Encoder
402
404
a b c d e i f g h j
Output of ENCODE function
10
PMA service interface
(3.125 million
code-groups/s per lane)
tx_code-group<9:0>
10 bits each on lanes 0:3
PMD service interface
(3.125 billion bits/s per lane)
bit 0 is transmitted first on each lane
tx_lane<0>
Output of DECODE function
PCS DECODE function
Input to DECODE function
0 0 1 1 1 1 1 x x x
Properly aligned comma+ symbol
0 1 2 3 4 5 6 7 8 9
rx_unaligned<9:0>
10 bits each on lanes 0:3
rx_lane<0>

FIG. 4

XGMII TXC	XGMII TXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36-2	See Table 36-2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character
NOTE—Values in TXD column are in hexadecimal.			

Table 36–2–Valid special code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj	Notes
K28.0	1C	000 11100	001111 0100	110000 1011	1
K28.1	3C	001 11100	001111 1001	110000 0110	1,2
K28.2	5C	010 11100	001111 0101	110000 1010	1
K28.3	7C	011 11100	001111 0011	110000 1100	1
K28.4	9C	100 11100	001111 0010	110000 1101	1
K28.5	BC	101 11100	001111 1010	110000 0101	2
K28.6	DC	110 11100	001111 0110	110000 1001	1
K28.7	FC	111 11100	001111 1000	110000 0111	1,2
K23.7	F7	111 10111	111010 1000	000101 0111	
K27.7	FB	111 11011	110110 1000	001001 0111	
K29.7	FD	111 11111	101110 1000	010001 0111	
K30.7	FE	111 11110	011110 1000	100001 0111	
NOTE 1 — Reserved. NOTE 2 — Contains a comma.					

FIG. 5

Code	Ordered_Set	Number of code-groups	Encoding
||I||	**Idle**		Substitute for XGMII Idle
||K||	Sync column	4	/K28.5/K28.5/K28.5/K28.5/
||R||	Skip column	4	/K28.0/K28.0/K28.0/K28.0/
||A||	Align column	4	/K28.3/K28.3/K28.3/K28.3/
	Encapsulation		
||S||	Start column	4	/K27.7/Dx.y/Dx.y/Dx.y/[a]
||T||	Terminate column	4	Terminate code-group in any lane
||T_0||	Terminate in Lane 0	4	/K29.7/K28.5/K28.5/K28.5/
||T_1||	Terminate in Lane 1	4	/Dx.y/K29.7/K28.5/K28.5/[a]
||T_2||	Terminate in Lane 2	4	/Dx.y/Dx.y/K29.7/K28.5/[a]
||T_3||	Terminate in Lane 3	4	/Dx.y/Dx.y/Dx.y/K29.7/[a]
	Control		
/E/	Error code-group	1	/K30.7/
	Link Status		
||Q||	Sequence ordered_set	4	/K28.4/Dx.y/Dx.y/Dx.y/[a]
||LF||	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
||RF||	Remote Fault signal	4	/K28.4/ D0.0/D0.0/D2.0/
||Qrsvd||	Reserved	4	||LF|| and ||RF||
	Reserved		
||Fsig||	Signal ordered_set	4	/K28.2/Dx.y/Dx.y/Dx.y/ [a,b]

[a]/Dx.y/ indicates any data code-group.
[b]/Reserved for INCITS T11.

FIG. 6

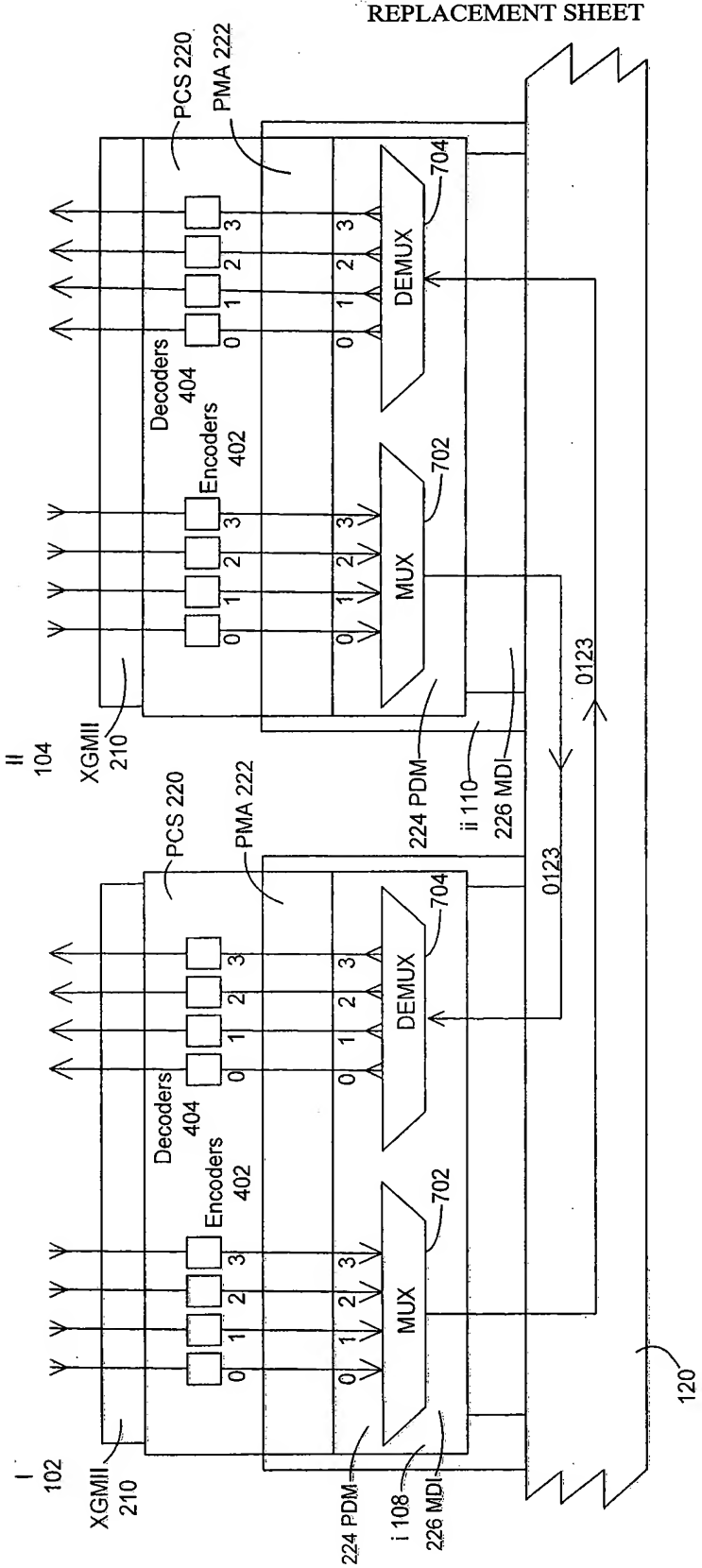
II
104
XGMII
210
PCS 220
PMA 222
Decoders
404
Encoders
402
DEMUX
704
MUX
702
0123
224 PDM
ii 110
226 MDI
I
102
i 108
120

FIG. 7A

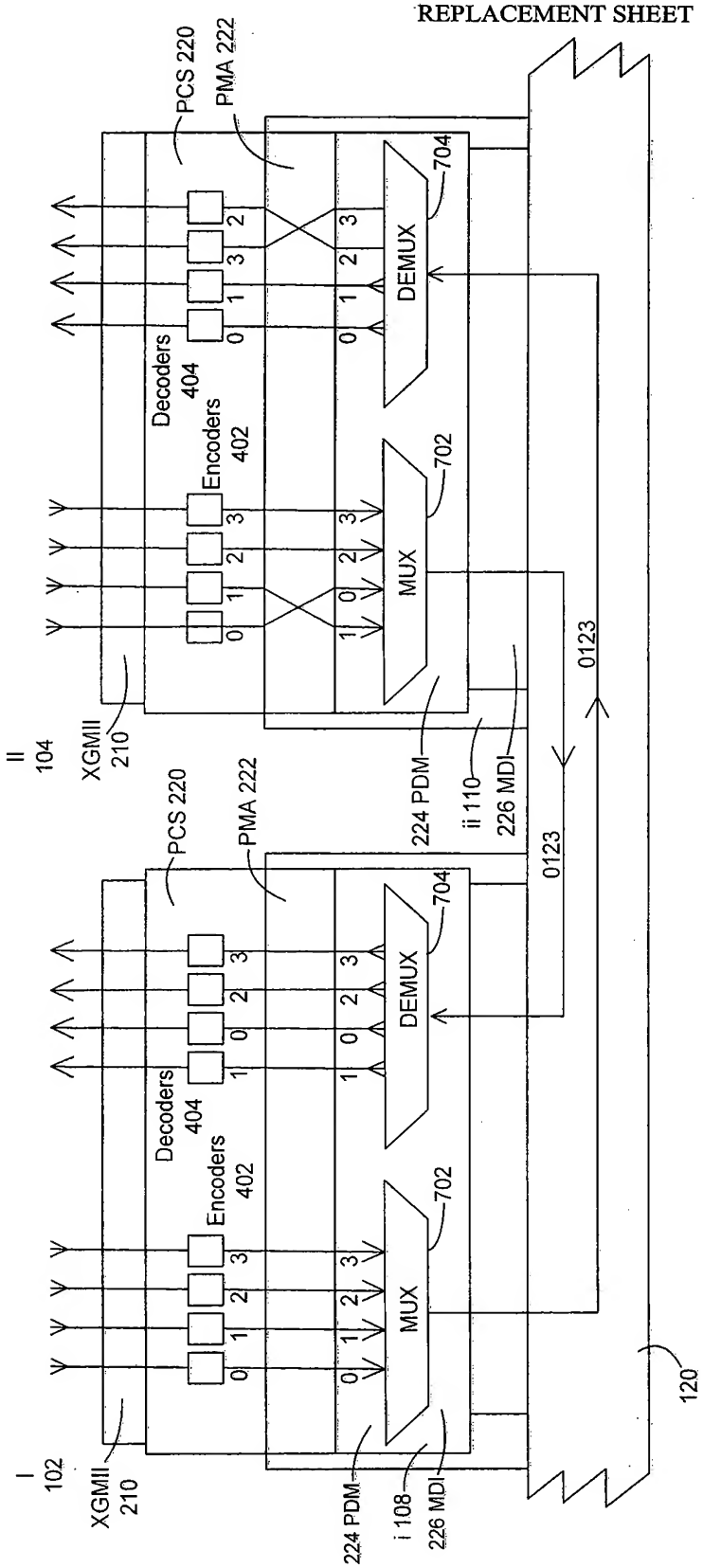
PCS 220
PMA 222
704
DEMUX
Decoders 404
Encoders 402
702
MUX
II 104
XGMII 210
224 PDM
ii 110
226 MDI
0123
I 102
i 108
120

FIG. 7B

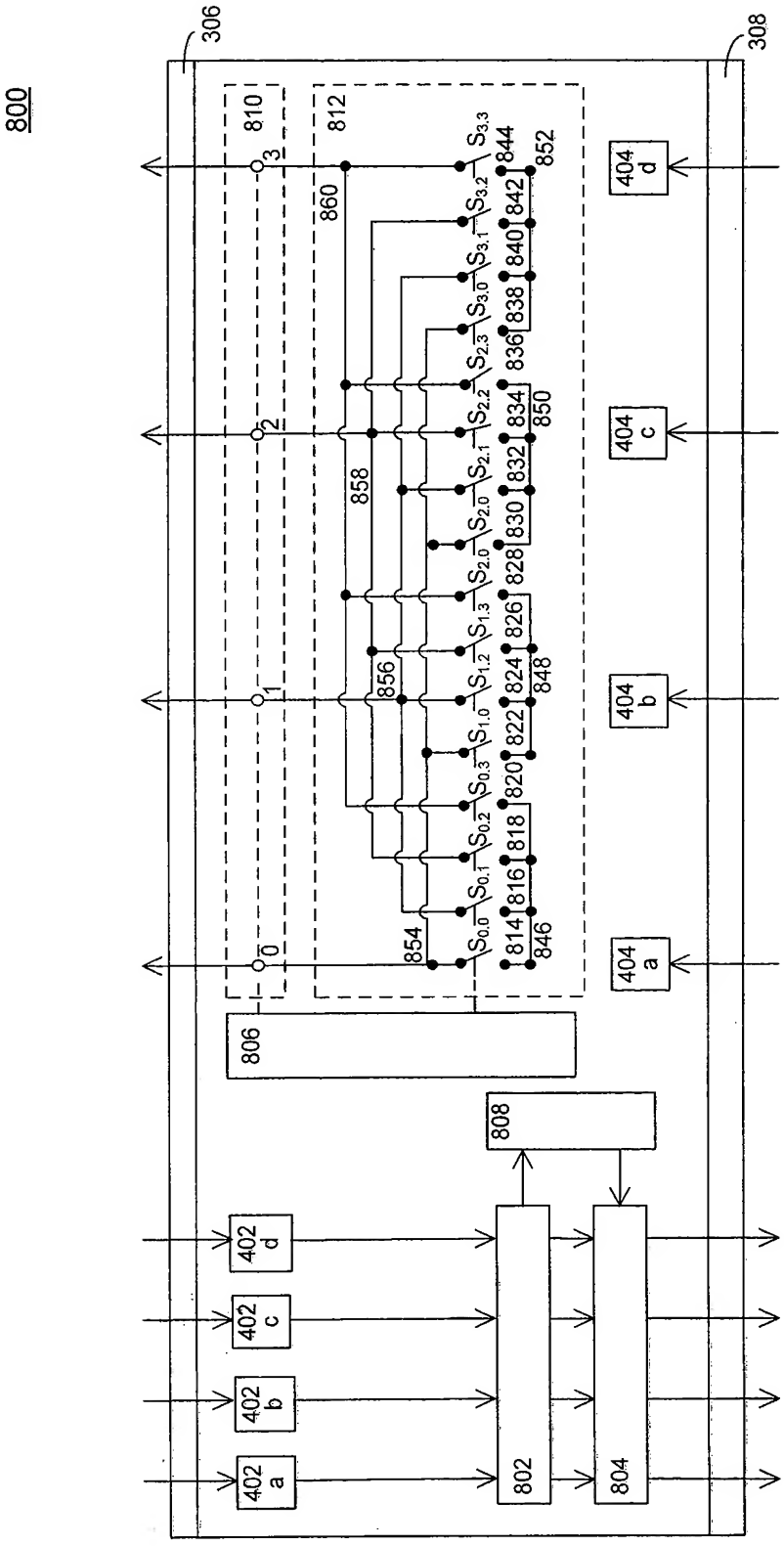
800
306
308
810
812
860
858
856
854
3
2
1
0
$S_{3.3}$
$S_{3.2}$
$S_{3.1}$
$S_{3.0}$
$S_{2.3}$
$S_{2.2}$
$S_{2.1}$
$S_{2.0}$
$S_{2.0}$
$S_{1.3}$
$S_{1.2}$
$S_{1.0}$
$S_{0.3}$
$S_{0.2}$
$S_{0.1}$
$S_{0.0}$
844
852
842
840
838
836
834
850
832
830
828
826
824
848
822
820
818
816
814
846
404 d
404 c
404 b
404 a
806
808
402 d
402 c
402 b
402 a
802
804

FIG. 8

Received Special Ordered Set	Lane Correction Switch Configuration
/Da.b/Dc.d/De.f/Dg.h/	/$S_{0.0}$/$S_{1.1}$/$S_{2.2}S_{3.3}$/
/Da.b/Dc.d/Dg.h/De.f/	/$S_{0.0}$/$S_{1.1}$/$S_{2.3}$/$S_{3.2}$/
/Da.b/De.f/Dc.d/Dg.h/	/$S_{0.0}$/$S_{1.2}$/$S_{2.1}$/$S_{3.3}$/
/Da.b/De.f/Dg.h/Dc.d/	/$S_{0.0}$/$S_{1.2}$/$S_{2.3}$/$S_{3.1}$/
/Da.b/Dg.h/Dc.d/De.f/	/$S_{0.0}$/$S_{1.3}$/$S_{2.1}$/$S_{3.2}$/
/Da.b/Dg.h/De.f/Dc.d/	/$S_{0.0}$/$S_{1.3}$/$S_{2.2}$/$S_{3.1}$/
/Dc.d/Da.b/De.f/Dg.h/	/$S_{0.1}$/$S_{1.0}$/$S_{2.2}$/$S_{3.3}$/
/Dc.d/Da.b/Dg.h/De.f/	/$S_{0.1}$/$S_{1.0}$/$S_{2.3}$/$S_{3.2}$/
/Dc.d/De.f/Da.b/Dg.h/	/$S_{0.1}$/$S_{1.2}$/$S_{2.0}$/$S_{3.3}$/
/Dc.d/De.f/Dg.h/Da.b/	/$S_{0.1}$/$S_{1.2}$/$S_{2.3}$/$S_{3.0}$/
/Dc.d/Dg.h/Da.b/De.f/	/$S_{0.1}$/$S_{1.3}$/$S_{2.0}$/$S_{3.2}$/
/Dc.d/Dg.h/De.f/Da.b/	/$S_{0.1}$/$S_{1.3}$/$S_{2.2}$/$S_{3.0}$/
/De.f/Da.b/Dc.d/Dg.h/	/$S_{0.2}$/$S_{1.0}$/$S_{2.1}$/$S_{3.3}$/
/De.f/Da.b/Dg.h/Dc.d/	/$S_{0.2}$/$S_{1.0}$/$S_{2.3}$/$S_{3.1}$/
/De.f/Dc.d/Da.b/Dg.h/	/$S_{0.2}$/$S_{1.1}$/$S_{2.0}$/$S_{3.3}$/
/De.f/Dc.d/Dg.h/Da.b/	/$S_{0.2}$/$S_{1.1}$/$S_{2.3}$/$S_{3.0}$/
/De.f/Dg.h/Da.b/Dc.d/	/$S_{0.2}$/$S_{1.3}$/$S_{2.0}$/$S_{3.1}$/
/De.f/Dg.h/Dc.d/Da.b/	/$S_{0.2}$/$S_{1.3}$/$S_{2.1}$/$S_{3.0}$/
/Dg.h/Da.b/Dc.d/De.f/	/$S_{0.3}$/$S_{1.0}$/$S_{2.1}$/$S_{3.2}$/
/Dg.h/Da.b/De.f/Dc.d/	/$S_{0.3}$/$S_{1.0}$/$S_{2.2}$/$S_{3.1}$/
/Dg.h/Dc.d/Da.b/De.f/	/$S_{0.3}$/$S_{1.1}$/$S_{2.0}$/$S_{3.2}$/
/Dg.h/Dc.d/De.f/Da.b/	/$S_{0.3}$/$S_{1.1}$/$S_{2.2}$/$S_{3.0}$/
/Dg.h/De.f/Da.b/Dc.d/	/$S_{0.3}$/$S_{1.2}$/$S_{2.0}$/$S_{3.1}$/
/Dg.h/De.f/Dc.d/Da.b/	/$S_{0.3}$/$S_{1.2}$/$S_{2.1}$/$S_{3.0}$/

FIG. 9

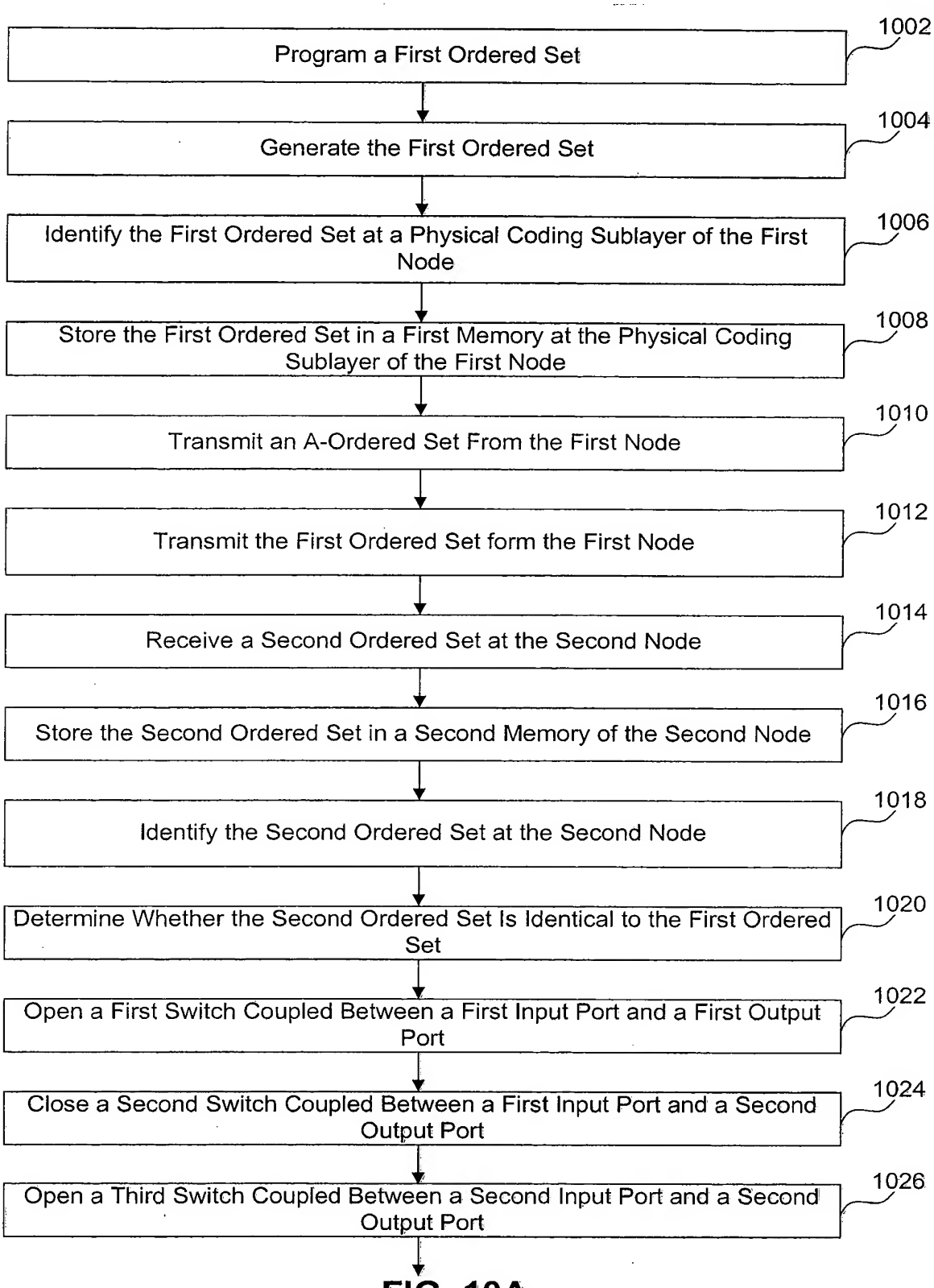
1000
Program a First Ordered Set
1002
Generate the First Ordered Set
1004
Identify the First Ordered Set at a Physical Coding Sublayer of the First Node
1006
Store the First Ordered Set in a First Memory at the Physical Coding Sublayer of the First Node
1008
Transmit an A-Ordered Set From the First Node
1010
Transmit the First Ordered Set form the First Node
1012
Receive a Second Ordered Set at the Second Node
1014
Store the Second Ordered Set in a Second Memory of the Second Node
1016
Identify the Second Ordered Set at the Second Node
1018
Determine Whether the Second Ordered Set Is Identical to the First Ordered Set
1020
Open a First Switch Coupled Between a First Input Port and a First Output Port
1022
Close a Second Switch Coupled Between a First Input Port and a Second Output Port
1024
Open a Third Switch Coupled Between a Second Input Port and a Second Output Port
1026

FIG. 10A

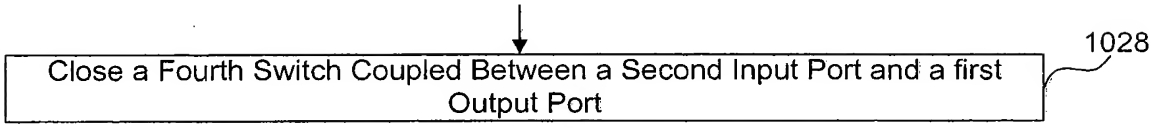
Close a Fourth Switch Coupled Between a Second Input Port and a first Output Port
1028

FIG. 10B

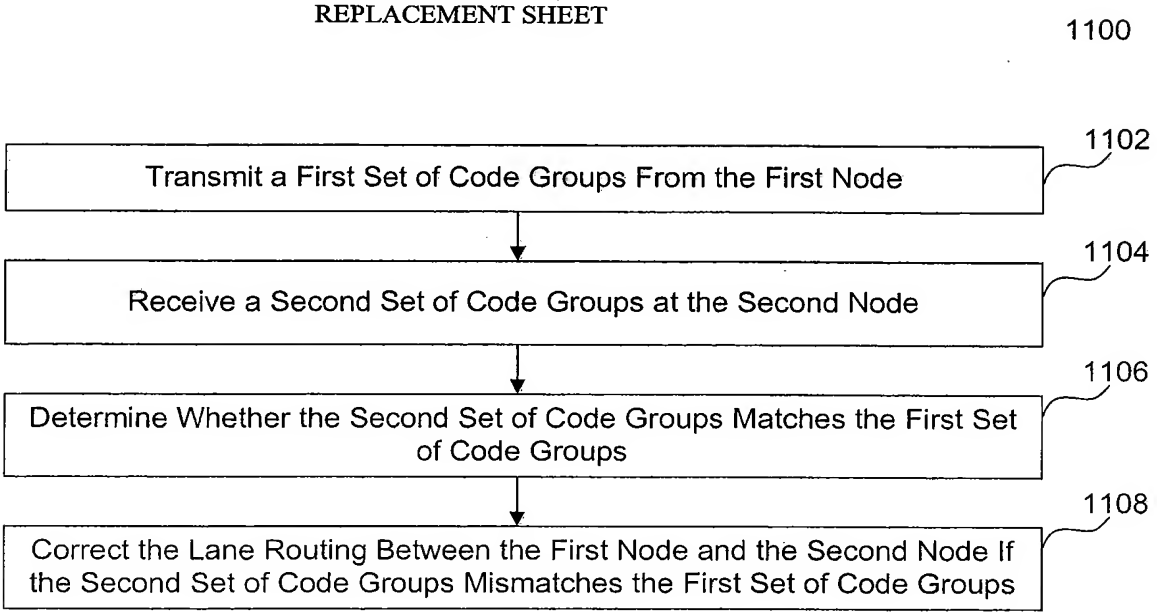
1100
Transmit a First Set of Code Groups From the First Node
1102
Receive a Second Set of Code Groups at the Second Node
1104
Determine Whether the Second Set of Code Groups Matches the First Set of Code Groups
1106
Correct the Lane Routing Between the First Node and the Second Node If the Second Set of Code Groups Mismatches the First Set of Code Groups
1108

FIG. 11